福建福盛达电子有限公司
Fujian Fushengda Electric Co.,LTD

APPROVAL SHEET
承 认 书

CUSTOMER 客户名称	
Part NO 产品型号	FSD090HF7016-A
Product type 产品内容	Mode: Transmissive type .Normally black. TFT LCD Module LCD Module: Graphic 720RGB*1280 Dot-matrix
Remarks 备注栏	□APPROVAL FOR SEPCIFICATIONS ONLY ■APPROVAL FOR SEPCIFICATIONS AND SAMPLE

LEAGEND LCM R&D CENTER：

Technical Department: 研发部门	Quality Assurance Department 质量保证部门	Approved by:核准
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Version	Revise Date	Page	Content	Modified by
V.1	2024-01-05	-	First Issued.	ZQF

Contents

1. General Specifications

9.0” is a color active matrix thin film transistor (TFT) IPS liquid crystal di splay (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, Driver IC, FPC and Backlight.

NO.	Item	Specification	Remark
1	Panel Size	9.0 inch(Diagonal)	
2	Driver Method	a-Si TFT active matrix	
3	Display Color	16.7M	
4	Display Mode	Normally Black	
5	Viewing Direction	All o’clock	
6	Resolution	720(RGB) x 1280	
7	Active Area	114.048(H) x 196.608(V) mm	
8	Dot Pitch	0.1584(H) x 0.1536(V) mm	
9	Pixel Arrangement	RGB stripe	
10	Module Size	125.80(W) x 210.00(H) x5.0(D) mm	
11	Interface	MIPI 4 lane	
12	Driving IC	FL7705N	
13	Luminance	TBD (TYP)	cd/m^2
14	Backlight	White LED	
15	Weight	TBD	g

Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: LCM weight tolerance: ±5%

2. Pin Assignment

No.	Symbol	Function	Remarks
1	NC	No connection	
2-3	VDD_1.8V	Power supply for the logic power and I/O circuit.	1.8V
4	NC	No connection	
5	RESET_1.8V	Global reset pin	1.8V
6	NC	No connection	
7	GND	Ground	
8	D0N	MIPI Date negative signal	
9	D0P	MIPI Date Positive signal	
10	GND	Ground	
11	D1N	MIPI Date negative signal	
12	D1P	MIPI Date Positive signal	
13	GND	Ground	
14	CLKN	MIPI CLK negative signal	
15	CLKP	MIPI CLK Positive signal	
16	GND	Ground	
17	D2N	MIPI Date negative signal	
18	D2P	MIPI Date Positive signal	
19	GND	Ground	
20	D3N	MIPI Date negative signal	
21	D3P	MIPI Date Positive signal	
22	GND	Ground	
23	NC	No connection	
24	AVDD	Power supply to the analog circuit.	9-12V
25-29	NC	No connection	
30	GND	Ground	

3. Operation Specifications

3.1. Absolute Maximum Ratings

Voltage (AGND=GND=0V, Ta = 25℃)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power Voltage	VDD	1.65	+3.6	V	
	AVDD	9	12	V	
Operating Temperature	Top	-20	60	℃	
Storage Temperature	Tst	-30	70	℃	

Note: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings case, the module may be permanently destroyed.

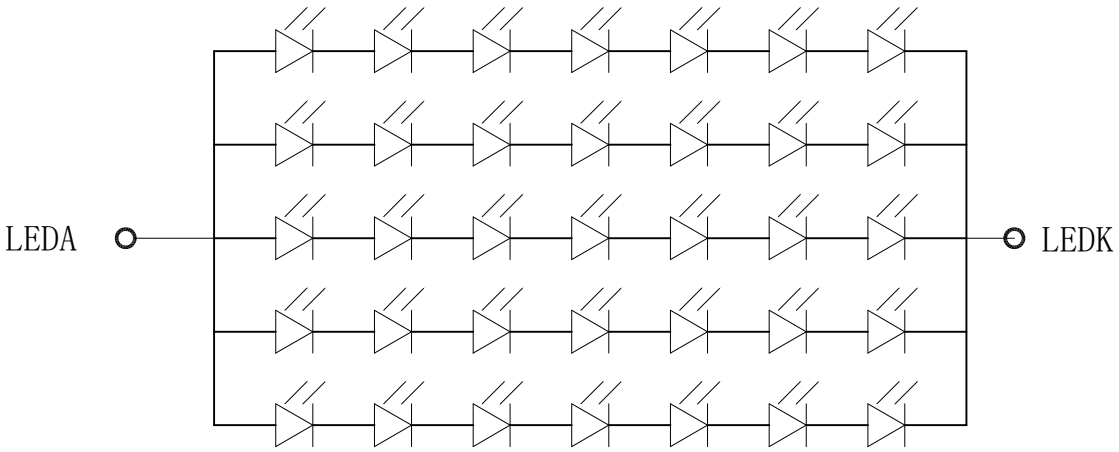
3.1.1. Typical Operation Range

Item	Symbol	values			Unit
		Min.	Typ.	Max.	
Power Voltage	VDD	1.65	1.8	3.6	V
Input logic high voltage	V_{IH}	0.7 V_{DD}	-	V_{DD}	V
Input logic low voltage	V_{IL}	0	-	0.3 V_{DD}	V

3.1.2. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply voltage of white LED backlight	V_L	21	22.4		V	
Current for LED backlight	I_L	-	100	-	mA	**20mA/LED**
Power dissipation	Pd		TBD		mW	35LED
Luminance (on the module surface,CA-410)			TBD	-	cd/m^2	
LED life time	-	20000	-	-	Hr	

LED CIRCUIT DIAGRAM



35 PCS LED Vled=22.4V ILed=100mA

3.2. Power Sequence

Power On Timing of External Power IC

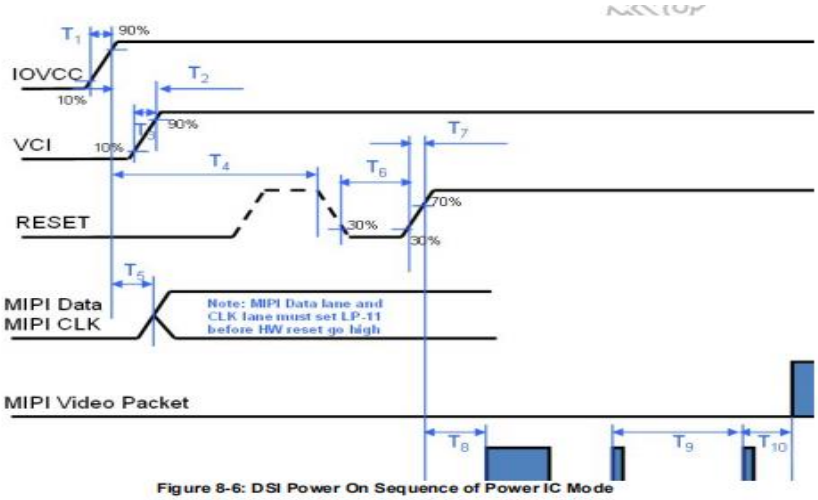


Figure 8-6: DSI Power On Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T1	0.01	-	10	ms
T2		No Limit		ms
T3	0.01	-	10	ms
T4	1	-	-	ms
T5	1	-	-	ms
T6	10	-	-	us
T7		No Limit		ns
T8	15	-	-	ms
T9	120	-	-	ms
T10		No Limit		ms
T11	100	150	-	ms

Table 8-1: DSI Power On Timing of Power IC Mode

Power Off Timing of External Power IC

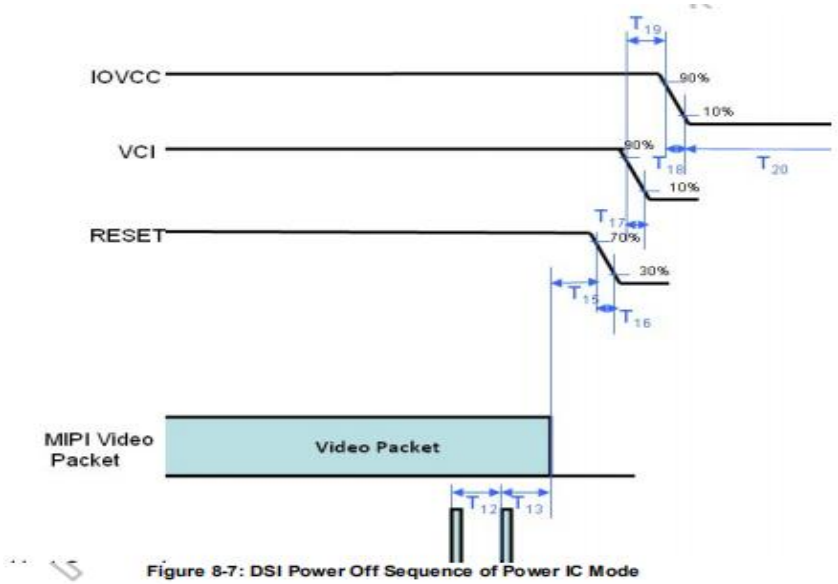


Figure 8-7: DSI Power Off Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T12	2	-	-	Frame
T13	2	-	-	Frame
T14	40	100	-	ms
T15	10	-	-	ms
T16		No Limit		ms
T17		No Limit		ms
T18		No Limit		ms
T19		No Limit		ms
T20	100			ms

Table 8-2: DSI Power Off Timing of Power IC Mode

3.3. Timing Characteristics

3.3.1. Mipi DC Electrical Characteristics

Basic Characteristics

External Power IC and PFM:

Parameter	Symbol	Conditions	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Power & Operating Voltages						
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Analog Operating voltage	VCI	Operation voltage	2.5	2.8	3.3	
Input / Output						
Logic High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Logic Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	μA
DC/DC Converter Operation						
VSP booster voltage	VSP	IVSP=1mA	4.5		6.2	V
VSN booster voltage	VSN	IVSN=-1mA	-6.2		-4.5	
VGH booster voltage	VGH	Ivgh=1mA	10		20	
VGL booster voltage	VGL	Ivgl=-1mA	-15		-7.5	
VGH and VGL difference	|VGH-VGL|	-	-	-	32	
Oscillator tolerance	OSC	25℃	-3		3	%
Source Driver						
Gamma reference voltage	VSPR	-	3.3		5.6	V
	VSNR	-	-5.6		-3.3	
Output voltage deviation	DVOS	VSSD+1.0 ~ VSPROUT-1.0	-	-	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VSPR-1.0 ~ VSPR-0.1V	-	-	+/- 50	mV
Output offset voltage	Voff	-		-	+/-50	mV
Standby Mode Current Consumption						
Sleep In Mode	VCI	Ta=25℃ VCI=2.8V IOVCC=1.8V	-	150	-	μA
	IOVCC		-	50	-	

3 Power Mode:

Parameter	Symbol	Conditions	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Power & Operating Voltages						
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Analog Operating voltage	VCI	Operation voltage	4.5		6.2	
Analog Operating voltage	VSP	Operation voltage	4.5		6.2	
Analog Operating voltage	VSN	Operation voltage	-6.2		-4.5	
Input / Output						
Logic High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Logic Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	μA
DC/DC Converter Operation						
VGH booster voltage	VGH	Ivgh=1mA	10		20	V
VGL booster voltage	VGL	Ivgl=-1mA	-15		-7.5	
VGH and VGL difference	|VGH-VGL|	-	-	-	32	
Oscillator tolerance	OSC	25℃	-3		3	%
Source Driver						
Gamma reference voltage	VSPR	-	3.3		5.6	V
	VSNR	-	-5.6		-3.3	
Output voltage deviation	DVOS	VSSD+1.0 ~ VSPROUT-1.0	-	-	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VSPR-1.0 ~ VSPR-0.1V	-	-	+/- 50	mV
Output offset voltage	Voff	-		-	+/-50	mV
Standby Mode Current Consumption						
Sleep In Mode	VSP	Ta=25℃ VSP=5.4V VSN=-5.4V IOVCC=1.8V	-	150	-	μA
	VSN		-	50	-	
	IOVCC		-	50	-	

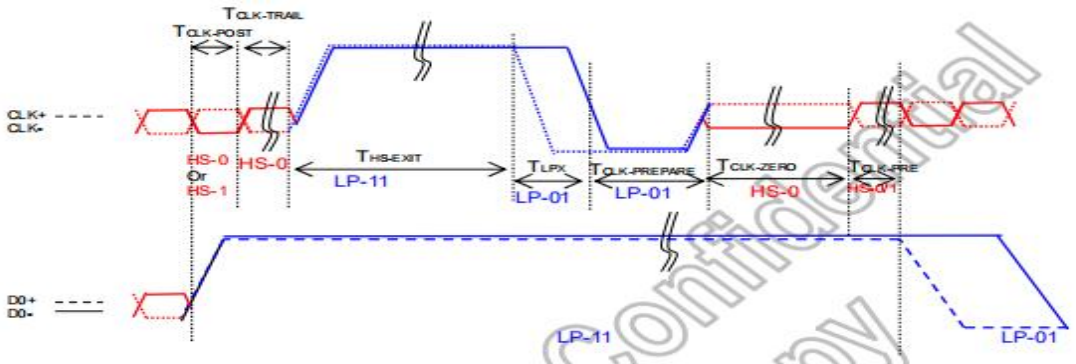
DSI DC Characteristics

LP Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps

Figure 7-1: Input glitch rejections of low-power receivers

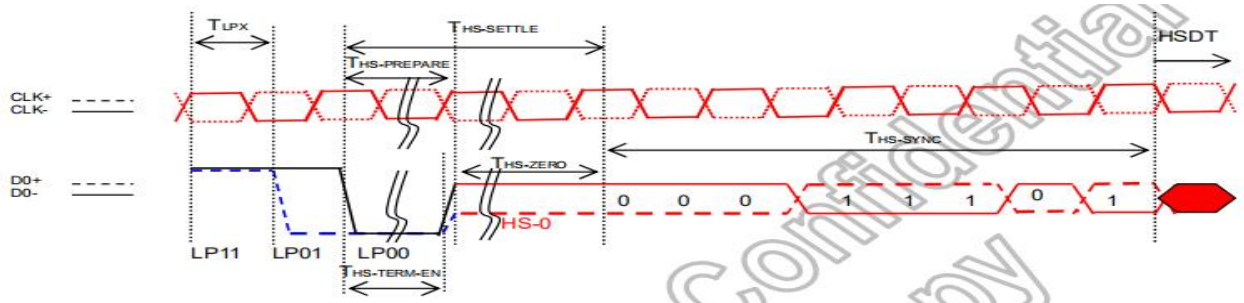
3.3.2. High Speed Clock Transmission



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7-7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

3.3.3. High Speed Data Transmission in Bursts



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

Table 7-5: DSI Low Power Mode to High Speed Mode Timing

4. Optical Specifications

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle		θT	CR≥10	-	80	-	degree	3
		θB		-	80	-		
		θL		-	80	-		
		θR		-	80	-		
Contrast Ratio		CR	Θ=0°	800	1000	-	-	4
Response Time		Ton+ Toff	25℃	-	30	35	ms	5
Chromaticity	White	X	LCM	-0.03	0.265	+0.03	-	1
		Y			0.265			
	Red	X	LCD SPEC	-0.03	0.666	+0.03		
		Y			0.326			
	Green	X			0.277			
		Y			0.587			
	Blue	X			0.136			
		Y			0.107			
Luminance (center)		L			TBD	-	cd/m²	1

Luminance Uniformity	ΔL		75	80	-	%	1.2

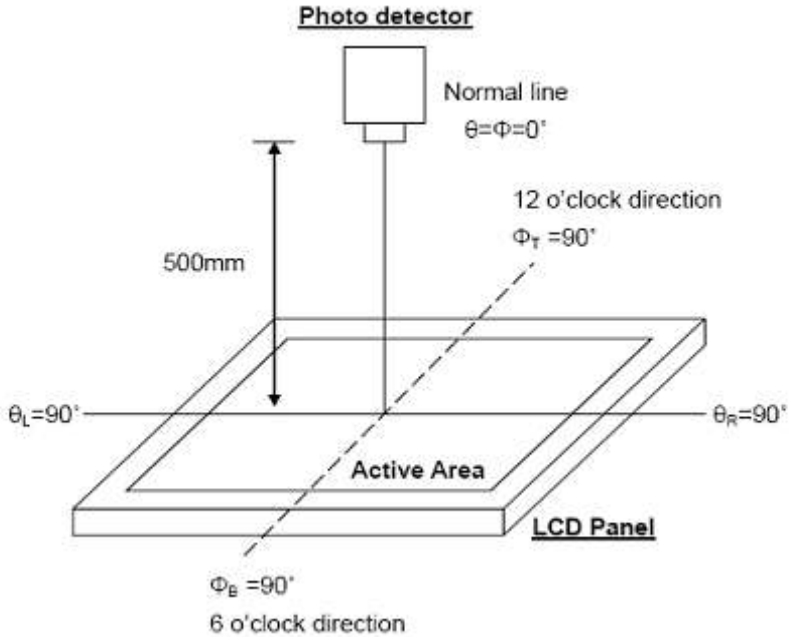
Note：The parameter is slightly changed by temperature, driving voltage and materiel

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment BM-7 (Φ8mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

The measured value is more than 5 minutes at the center point of the LCD panel, and the backlight is turned on at the same time.

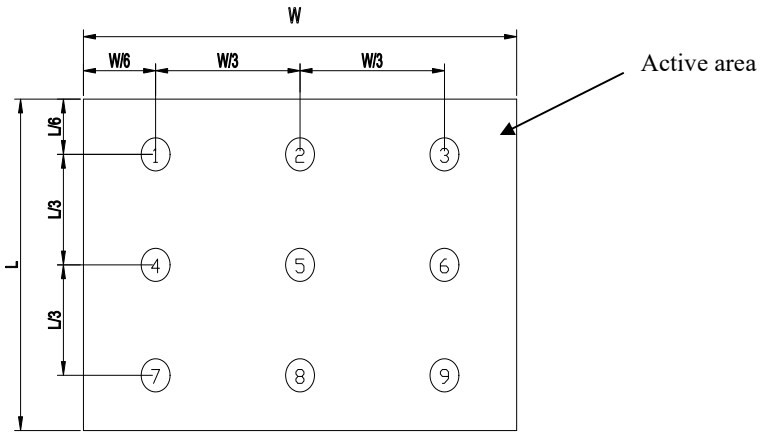


Note 2: The luminance uniformity is calculated by using following formula.

⊿Bp = Bp (Min.) / Bp (Max.)×100 (%)

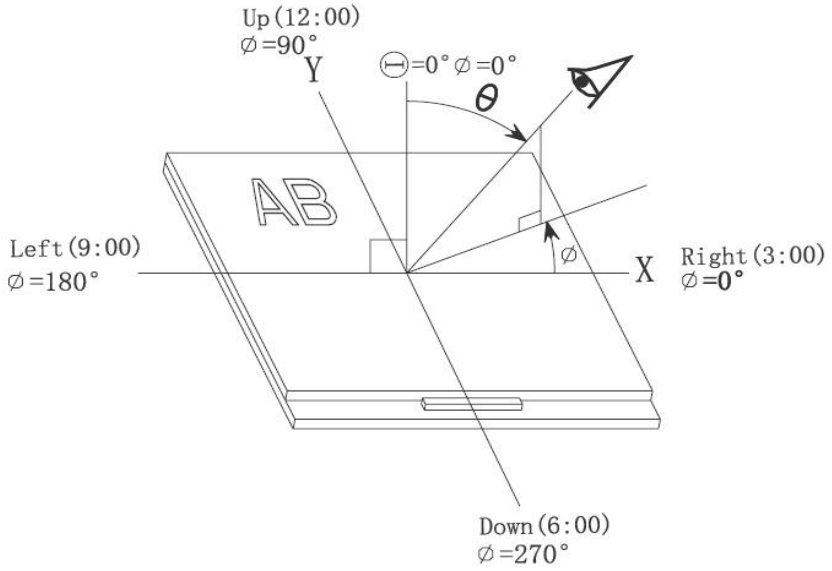
Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.



Note 3: The definition of viewing angle:

Refer to the graph below marked by θ and Φ



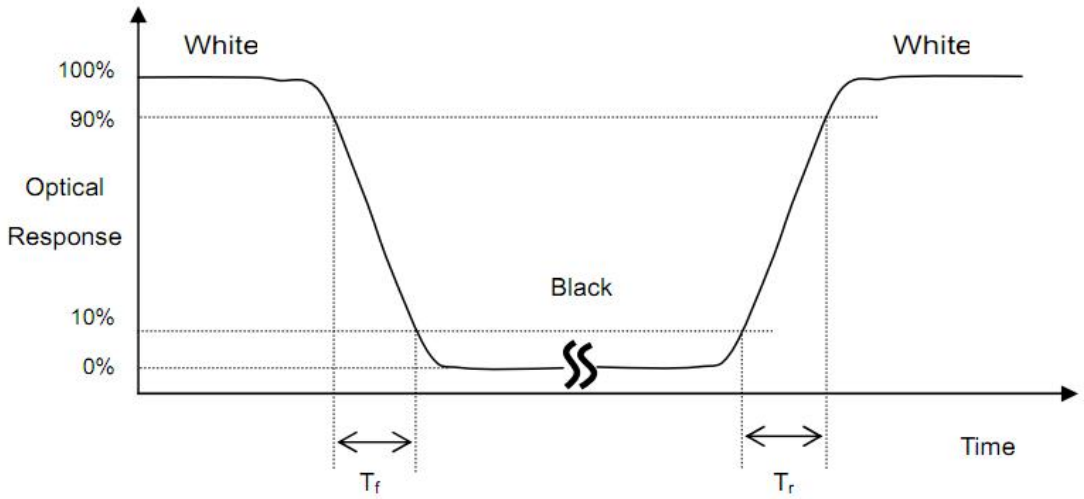
Note 4: Definition of contrast ratio

Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 5: Definition of Response time

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(Tf) and from “white” to “black”(Tr), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



5. Reliability Test Items

Item	Test Conditions	Remark
High Temperature Storage	Ta=70℃;96Hrs	Note1 ,Note4
Low Temperature Storage	Ta=-30℃;96Hrs	Note1, Note4
High Temperature Operation	Ts=60℃;96Hrs	Note2 ,Note4
Low Temperature Operation	Ts=-20℃;96Hrs	Note4
Operation at High Temperature and Humidity	+50℃,85%RH;96Hrs (no condensation)	Note4
Thermal Shock	-20℃/30min~+60℃/30min for a total 10 cycles	Start with cold temperature and end with high temperature
Package Drop Test	Height 60cm 1corner ， 3edges ， 6surfaces	
Elector Static Discharge	150pF/330Ω, Contact:±4KV,Air:±8KV	Human Body Mode
Image Sticking	25℃ ；1hrs	Note5

Note1: Ta is the ambient temperature of samples.

Note2: Ts is the temperature of panel's surfaces.

Note3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

Note4: before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note5: Condition of image sticking test :25℃±2℃, Operation with test pattern sustained for 1hrs,then change to gray pattern immediately. after 5 mins, the mura must be disappeared completely.

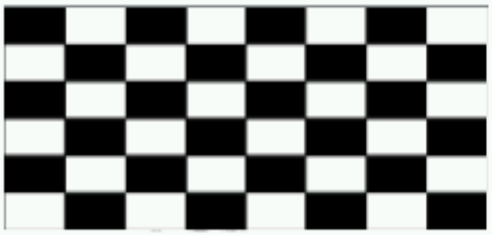


Image Sticking -pattern

Lv127 Gray pattern

6. Mechanical Drawing